



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,111	12/01/2003	Yoshio Okayama	65933-056	9924
20277	7590	09/21/2005	EXAMINER	
MCDERMOTT WILL & EMERY LLP			GURLEY, LYNNE ANN	
600 13TH STREET, N.W.			ART UNIT	
WASHINGTON, DC 20005-3096			PAPER NUMBER	
			2812	

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/724,111

Applicant(s)

OKAYAMA ET AL.

Examiner

Lynne A. Gurley

Art Unit

2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 11 August 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

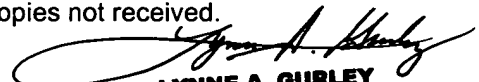
**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 December 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.



**LYNNE A. GURLEY**  
**PRIMARY PATENT EXAMINER**  
**TC 2800, AU 2812**

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

This Office action is in response to the RCE with remarks, filed 8/11/05.

Currently, claims 1-20 are pending.

#### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/11/05 has been entered.

#### ***Priority***

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

#### ***Drawings***

2. The drawings are objected to because Figures 1A-1D and 2A-2D should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing

Art Unit: 2812

should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Specification.***

3. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the limitation regarding “a connection plug” (claim 2 in the paragraph describing the first polishing step).
4. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

***Claim Rejections - 35 USC § 112***

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Art Unit: 2812

6. Claims 2, 5-6, 8, 11-12, 14, and 17-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claims 2, 8 and 14 recite the limitation "said first interconnection" in line 6. There is insufficient antecedent basis for this limitation in the claim.

Claims 5-6, 11-12 and 17-18 are indefinite in that the step of forming a via hole reaching an upper surface of the first interconnection cannot be realized since only the insulating film and the sacrificial film have been selectively removed. The diffusion barrier is still in place since it is not included in the removal step, so that the via hole cannot reach the upper surface of the first interconnection.

***Claim Rejections - 35 USC § 102***

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-3 and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Stamper et al. (US 6,838,355, dated 1/4/05, filed 8/4/03).

Stamper shows the method as claimed in figures 3 and 4 and corresponding text, as forming a diffusion barrier film 42 (SiN or SiC) on a semiconductor substrate 40 (having lower level wirings and interconnects and devices for connection to the interconnect within; col. 10,

Art Unit: 2812

lines 33-41) and then forming an insulating film 43 on the diffusion barrier film, forming a concave 44a/b (in fig. 4(c), the concave is formed through the barrier) in the insulating film by selectively removing the insulating film and the diffusion barrier film, and then forming a metal film 44 filling the concave; conducting a first polishing over a whole surface of the substrate to form a metal area filled in the concave (fig. 4(c); Planarization is performed by CMP (column 11, lines 22-27); and conducting a second polishing over the whole surface of the substrate to remove parts of the metal area and of the insulating film (fig. 4(e)); wherein the second polishing also removed a part of a normal taper formed in an upper part of the concave (column 11, lines 53-67; column 12, lines 1-10).

Stamper also shows the method as in claims 2, 3 and 5, in figure 3, with diffusion barrier 32; substrate 30 (with lower level wirings and interconnects and devices for connection to the interconnection within); insulating film 33; sacrificial layer 34 (column 8, lines 22-67; column 9, lines 1-67; column 10, lines 1-31); metal film 35; first polishing (fig. 3 (c) ); Planarization is performed by CMP (column 9, lines 36-42) and second polishing (figs. 3(d) 3(e)).

10. Claims 1-2 are rejected under 35 U.S.C. 102(e) as being anticipated by Seta et al. (US 6,605,542, dated 8/12/03, filed 11/29/01).

Seta shows the method as claimed in figure 6, especially, with diffusion barrier film 4, insulating film 2, via hole 5, interconnection trench 8, first interconnection 3, metal film 3a, wherein a two step CMP is performed (column 17, lines 16-26 especially. See column 16, line 4,

Art Unit: 2812

fourth embodiment also). Note that the connection plug is considered to be where the via and interconnection plug meet.

11. Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by You et al. (US 6,756,672, dated 6/29/04, filed 2/6/01).

You shows the method as claimed in figures 2 and 5 and corresponding text, as forming a diffusion barrier film 111 on a semiconductor substrate (having a lower level wiring 111) and then forming an insulating film 112-142 on the diffusion barrier film, forming a concave 146/116 (in fig. 5(I), the concave is formed through the barrier) in the insulating film by selectively removing the insulating film and the diffusion barrier film, and then forming a metal film 120/122 filling the concave; conducting a first polishing over a whole surface of the substrate to form a metal area filled in the concave (fig. 5(K) and 5(L)); Planarization is performed by CMP; and conducting a second polishing over the whole surface of the substrate to remove parts of the metal area and of the insulating film (fig. 5K and 5L); wherein the second polishing also removed a part of a normal taper formed in an upper part of the concave (Fig 5L). A sacrificial layer 113 is used. Figure 5L shows the normal taper removed in both 113 and 142.

### ***Claim Rejections - 35 USC § 103***

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Art Unit: 2812

13. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

14. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

15. Claims 7-9, 11, 13-15, 17 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stamper et al. (US 6,838,355, dated 1/4/05, filed 8/4/03) in view of Sameshima et al (US 2003/0203624, dated 10/30/03, filed 3/24/03).

Stamper shows the method substantially as claimed and as described in the preceding paragraphs.

Stamper lacks anticipation only in not teaching that the information on a polishing rate I the second polishing is obtained and on a basis of the information, and end point of the second polishing is determined; a thickness of the insulating film polished along with the metal is observed to determine an end point of the second polishing; a thickness of the insulating film



Art Unit: 2812

polished along with the second interconnection is observed to determine an end point of the second polishing; the step of conducting the first polishing comprises using a slurry containing an oxidizing agent; and, that the step of conducting the second polishing comprises using a slurry containing abrasive grains and a corrosion inhibitor.

Sameshima teaches, in a similar planarized dual damascene structure, with emphasis on figure 7 and corresponding text for the dual damascene structure (a trench and a via), a diffusion barrier layer 713/714 on a semiconductor substrate 710 and, an insulating film on the diffusion barrier and, 2 step polishing method of a substrate with multi-layer interconnection, with a dual damascene interconnect 729/730 connecting to an underlying first interconnection 719. The dual damascene interconnect is filled with metal 732 and then a two step polishing process is conducted to planarize the structure (figs. 7D-7F; [0091]-[0100]). Sameshima also discusses corrosion inhibitors, abrasives and end point detection based on thickness of the film per unit time and its effect on the polishing rate [0005].

It would have been obvious to one of ordinary skill in the art to have used the above-mentioned, claimed end point detection methods, and slurry contents, in the method of Stamper, with the motivation that Sameshima teaches that thicknesses of layers and information regarding polishing rates of materials are conventionally used for end point detection purposes, and additionally, with the motivation that the oxidizing agents and abrasive grains and corrosion inhibitors are also conventionally well known, as taught in Sameshima, and effectively used in slurries for exemplary planarization.

Art Unit: 2812

16. Claims 7-8, 13-14, and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seta et al. (US 6,605,542, dated 8/12/03, filed 11/29/01) in view of Sameshima et al (US 2003/0203624, dated 10/30/03, filed 3/24/03).

Seta shows the method substantially as claimed and as described in the preceding paragraphs.

Seta lacks anticipation only in not teaching that the information on a polishing rate I the second polishing is obtained and on a basis of the information, and end point of the second polishing is determined; a thickness of the insulating film polished along with the metal is observed to determine an end point of the second polishing; a thickness of the insulating film polished along with the second interconnection is observed to determine an end point of the second polishing; the step of conducting the first polishing comprises using a slurry containing an oxidizing agent; and, that the step of conducting the second polishing comprises using a slurry containing abrasive grains and a corrosion inhibitor.

Sameshima teaches, in a similar planarized dual damascene structure, with emphasis on figure 7 and corresponding text for the dual damascene structure (a trench and a via), a diffusion barrier layer 713/714 on a semiconductor substrate 710 and, an insulating film on the diffusion barrier and, 2 step polishing method of a substrate with multi-layer interconnection, with a dual damascene interconnect 729/730 connecting to an underlying first interconnection 719. The dual damascene interconnect is filled with metal 732 and then a two step polishing process is conducted to planarize the structure (figs. 7D-7F; [0091]-[0100]). Sameshima also discusses corrosion inhibitors, abrasives and end point detection based on thickness of the film per unit time and its effect on the polishing rate [0005].

Art Unit: 2812

It would have been obvious to one of ordinary skill in the art to have used the above-mentioned, claimed end point detection methods, and slurry contents, in the method of Seta, with the motivation that Sameshima teaches that thicknesses of layers and information regarding polishing rates of materials are conventionally used for end point detection purposes, and additionally, with the motivation that the oxidizing agents and abrasive grains and corrosion inhibitors are also conventionally well known, as taught in Sameshima, and effectively used in slurries for exemplary planarization.

17. Claims 7-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over You et al. (US 6,756,672, dated 6/29/04, filed 2/6/01) in view of Sameshima et al (US 2003/0203624, dated 10/30/03, filed 3/24/03).

You shows the method substantially as claimed and as described in the preceding paragraphs. Additionally, You shows that an abrasive ( $\text{Al}_2\text{O}_3$ ) is used in the slurry.

You lacks anticipation only in not teaching that the information on a polishing rate I the second polishing is obtained and on a basis of the information, and end point of the second polishing is determined; a thickness of the insulating film polished along with the metal is observed to determine an end point of the second polishing; a thickness of the insulating film polished along with the second interconnection is observed to determine an end point of the second polishing; the step of conducting the first polishing comprises using a slurry containing an oxidizing agent; and, that the step of conducting the second polishing comprises using a slurry containing abrasive grains and a corrosion inhibitor.

Sameshima teaches, in a similar planarized dual damascene structure, with emphasis on figure 7 and corresponding text for the dual damascene structure (a trench and a via), a diffusion barrier layer 713/714 on a semiconductor substrate 710 and, an insulating film on the diffusion barrier and, 2 step polishing method of a substrate with multi-layer interconnection, with a dual damascene interconnect 729/730 connecting to an underlying first interconnection 719. The dual damascene interconnect is filled with metal 732 and then a two step polishing process is conducted to planarize the structure (figs. 7D-7F; [0091]-[0100]). Sameshima also discusses corrosion inhibitors, abrasives and end point detection based on thickness of the film per unit time and its effect on the polishing rate [0005].

It would have been obvious to one of ordinary skill in the art to have used the above-mentioned, claimed end point detection methods, and slurry contents, in the method of You, with the motivation that Sameshima teaches that thicknesses of layers and information regarding polishing rates of materials are conventionally used for end point detection purposes, and additionally, with the motivation that the oxidizing agents and abrasive grains and corrosion inhibitors are also conventionally well known, as taught in Sameshima, and effectively used in slurries for exemplary planarization.

### ***Response to Arguments***

18. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

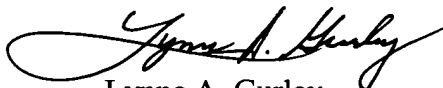
***Conclusion***

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See the PTO Form 892. Also, see Lukanc et al. 6,117,782 from previous 892 for support concerning removal of sacrificial layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynne A. Gurley whose telephone number is 571-272-1670. The examiner can normally be reached on M-F 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Lynne A. Gurley  
Primary Patent Examiner  
TC 2800, Art Unit 2812

LAG  
September 15, 2005